REMARKS

Claims 1-52, as amended, remain herein. Claims 23-52 remain herein but are presently withdrawn from consideration.

The claims as amended herein and the following remarks are responsive to the final Office Action mailed January 2, 2004.

Applicants appreciate the statements in the Office Action that claims 4, 6-11, 15 and 17-22 would be allowable if rewritten in independent form to include all of the limitations of the independent claim(s) from which they depend.

Minor, editorial changes have been made in claims 1-22.

1. Objections were stated to claims 1-22. Each informality has been amended, thereby mooting those objections.

2. Claims 1 and 12 were rejected under 35 U.S.C. §102(e) over Rohrbaugh et al. U.S. Patent 6,067,651.

The presently claimed fault detecting method includes detecting faults in a circuit to which a fault list corresponds, wherein the fault list corresponds to at least one of (a) information identifying "physical sites" on a physical layout of

a semiconductor integrated circuit where a possible fault is likely to occur, and (b) information required to reduce faults, and detecting faults in accordance with the fault list. This method is nowhere disclosed or suggested in the cited reference.

The Office Action cites Rohrbaugh '651, column 2, lines 15-20, as allegedly disclosing information identifying locations of a semiconductor integrated circuit where a possible fault is likely to occur. However, Rohrbaugh '651 does not disclose detecting faults in a circuit having a related fault list, wherein the fault list corresponds to (a) information identifying "physical sites" on a physical layout of a semiconductor integrated circuit where a possible fault is likely to occur and (b) information required to reduce faults. Such fault would be an improper operation due to a short-circuit between lines caused by foreign matter adhered between adjacent lines or due to signals (cross-talk) between the lines.

While Rohrbaugh '651 discusses "modeling", Rohrbaugh '651 does not describe "modeling" as referring to the actual physical layout of the circuit. Instead, Rohrbaugh '651, column 5, lines 22-35, describes device model 108 as comprising data for logic

and connectivity, and also physical structure of devices in the circuit. Such logic and connectivity describes point-to-point connections, which is completely different from actual routes real conductors trace across the silicon. There is no mention of the related physical structure of the physical layout of the actual circuit on silicon. Rohrbaugh '651 does not disclose a fault detecting method comprising using information identifying physical sites of the physical layout of a semiconductor integrated circuit. Further, none of the figures of Rohrbaugh '651 show any mechanism for collecting or providing such physical layout description.

For the foregoing reasons, Rohrbaugh '651 fails to disclose all elements of applicants' claimed invention, and therefore is not a proper basis for rejection under §102. And, there is no disclosure or teaching in Rohrbaugh '651 that would have suggested the desirability of modifying any portions thereof effectively to anticipate or suggest applicants' presently claimed invention. Accordingly, reconsideration and withdrawal of this rejection are respectfully requested.

3. Claims 2 and 13 were rejected under 35 U.S.C. §103(a) over Rohrbaugh '651 and Goel U.S. Patent 4,204,633, and claims 3, 5, 14 and 16 were rejected under 35 U.S.C. §103(a) over Rohrbaugh '651 and Publication No. NN9205250, "Improved Method for Weighted Random Pattern Weight Generation," 18M Technical Disclosure Bulletin, May 1992, U.S.

Contrary to statements in the Office Action, Rohrbaugh '651 does not disclose a fault detecting method comprising using information identifying physical sites of the physical layout of a semiconductor integrated circuit, as discussed herein in relation to claims 1 and 12, from which claims 2 and 13, respectively, depend. Therefore, claims 2 and 13 are allowable for the same reasons discussed above herein for claims 1 and 12.

The Office Action cites Goel '633 as allegedly teaching omitting possible faults that are difficult to detect from the fault list, i.e., possible faults having a specified low probability of occurrence from the fault list, as presently recited in claims 2 and 13. Goel '633 discloses that a control counter is provided for simulation of faults and when the count exceeds a specific value, the simulation is stopped. Such

disclosure relates merely to processing control, but does not relate to deleting low probability of occurring faults from a fault list, as recited in applicants' claims 2 and 13.

Additionally, while Rohrbaugh '651 discloses modeling in connection with test sequences, Rohrbaugh '651 does not disclose modeling regarding determining the likelihood of a fault occurring at a "physical site on a physical layout" of a semiconductor integrated circuit, as discussed herein.

For the foregoing reasons, neither Rohrbaugh '651 nor Goel '633 contains any teaching, suggestion, reason, motivation or incentive that would have led one of ordinary skill in the art to applicants' claimed invention. Nor is there any disclosure or teaching in either of these references that would have suggested the desirability of combining any portions thereof effectively to anticipate or suggest applicants' presently claimed invention. Claims 2, 3 and 5, which depend from claim 1, and claims 13, 14 and 16, which depend from claim 12, are allowable for the same reasons as claims 1 and 12. Accordingly, reconsideration and withdrawal of this rejection are respectfully requested.

All claims 1-52 are now proper in form and patentably distinguished over all grounds of rejection stated in the Office Action. Accordingly, allowance of all claims 1-52 is respectfully requested.

Should the Examiner deem that any further action by the applicants would be desirable to place this application in even better condition for issue, the Examiner is requested to telephone applicants' undersigned representatives.

Respectfully submitted,

PARKHURST & WENDEL, L.L.P.

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Date

Roger W. Parkhurst
Registration No. 25,177
Robert N. Wieland
Registration No. 40,225

RWP:RNW/mhs

Attorney Docket No.: YMOR:186

PARKHURST & WENDEL, L.L.P.
1421 Prince Street, Suite 210
Alexandria, Virginia 22314-2805
Telephone: (703) 739-0220